

## WHAT IS CLAIMED IS:

1       1. A bus interface unit for transferring data between a  
2 plurality of bus devices, said bus interface unit comprising:

3           1) a first bus device interface comprising: a) a first  
4 incoming request bus for receiving request packets from a first one  
5 of said plurality of bus devices; b) a first outgoing request bus  
6 for transmitting request packets to said first bus device; c) a  
7 first incoming data bus for receiving data packets from said first  
8 bus device; and d) a first outgoing data bus for transmitting data  
9 packets to said first bus device;

10           2) a second bus device interface comprising: a) a second  
11 incoming request bus for receiving request packets from a second  
12 one of said plurality of bus devices; b) a second outgoing request  
13 bus for transmitting request packets to said second bus device;  
14 c) a second incoming data bus for receiving data packets from said  
15 second bus device; and d) a second outgoing data bus for  
16 transmitting data packets to said second bus device; and

17           3) an arbitration circuit capable of determining a first  
18 priority level associated with a first request packet received from  
19 said first bus device and capable of determining a second priority  
20 level associated with a second request packet received from said  
21 second bus device.

1       2. The bus interface unit as set forth in Claim 1 wherein  
2       said arbitration circuit compares said first priority level and  
3       said second priority level to determine which of said first and  
4       second priority levels is higher.

1       3. The bus interface unit as set forth in Claim 2 wherein  
2       said arbitration circuit, in response to a determination that said  
3       first priority level is higher than said second priority level,  
4       causes said bus interface unit to process said first request packet  
5       prior to processing said second request packet.

1       4. The bus interface unit as set forth in Claim 2 wherein  
2       said arbitration circuit, in response to a determination that said  
3       first priority level is equal to said second priority level, causes  
4       said bus interface unit to process said first and second request  
5       packets on a rotating turn basis.

1       5. The bus interface unit as set forth in Claim 1 further  
2       comprising a time slice timer capable of producing a current time  
3       slice value.

1       6. The bus interface unit as set forth in Claim 5 wherein  
2 said arbitration circuit is capable of determining a fixed time  
3 slice range associated with said first bus device and comparing  
4 said fixed time slice range with said current time slice value.

1       7. The bus interface unit as set forth in Claim 6 wherein  
2 said arbitration circuit, in response to a determination that said  
3 current time slice value is within said fixed time slice range,  
4 causes said bus interface unit to process said first request packet  
5 prior to processing said second request packet.

1       8. The bus interface unit as set forth in Claim 7 wherein  
2 said arbitration circuit, in response to a determination that said  
3 current time slice value is within said fixed time slice range,  
4 causes said bus interface unit to process said first request packet  
5 prior to processing any pending request packet received by said bus  
6 interface unit.

1           9. An integrated circuit data comprising:

2           1) N bus devices capable of transferring data with one  
3 another; and

4           2) a bus interface unit for transferring data between  
5 said N bus devices, said bus interface unit comprising:

6           a) N bus interfaces, each of said N bus interfaces  
7 comprising: i) an incoming request bus for receiving request  
8 packets from one of said N bus devices; ii) an outgoing  
9 request bus for transmitting request packets to said one of  
10 said N bus devices; iii) an incoming data bus for receiving  
11 data packets from said one of said N bus devices; and iv) an  
12 outgoing data bus for transmitting data packets to said one of  
13 said N bus devices; and

14           b) an arbitration circuit capable of determining a  
15 first priority level associated with a first request packet  
16 received from a first bus device and capable of determining a  
17 second priority level associated with a second request packet  
18 received from a second bus device.

1       10. The integrated circuit as set forth in Claim 9 wherein  
2       said arbitration circuit compares said first priority level and  
3       said second priority level to determine which of said first and  
4       second priority levels is higher.

1       11. The integrated circuit as set forth in Claim 10 wherein  
2       said arbitration circu

3               it, in response to a determination that said first priority  
4       level is higher than said second priority level, causes said bus  
5       interface unit to process said first request packet prior to  
6       processing said second request packet.

1       12. The integrated circuit as set forth in Claim 10 wherein  
2       said arbitration circuit, in response to a determination that said  
3       first priority level is equal to said second priority level, causes  
4       said bus interface unit to process said first and second request  
5       packets on a rotating turn basis.

1       13. The integrated circuit as set forth in Claim 9 further  
2       comprising a time slice timer capable of producing a current time  
3       slice value.

1        14. The integrated circuit as set forth in Claim 13 wherein  
2        said arbitration circuit is capable of determining a fixed time  
3        slice range associated with said first bus device and comparing  
4        said fixed time slice range with said current time slice value.

1        15. The integrated circuit as set forth in Claim 14 wherein  
2        said arbitration circuit, in response to a determination that said  
3        current time slice value is within said fixed time slice range,  
4        causes said bus interface unit to process said first request packet  
5        prior to processing said second request packet.

1        16. The integrated circuit as set forth in Claim 15 wherein  
2        said arbitration circuit, in response to a determination that said  
3        current time slice value is within said fixed time slice range,  
4        causes said bus interface unit to process said first request packet  
5        prior to processing any pending request packet received by said bus  
6        interface unit.

1        17. For use in a bus interface unit comprising N bus  
2 interfaces, each of the N bus interfaces comprising: i) an incoming  
3 request bus for receiving request packets from a corresponding one  
4 of N bus devices; ii) an outgoing request bus for transmitting  
5 request packets to the corresponding bus device; iii) an incoming  
6 data bus for receiving data packets from the corresponding bus  
7 device; and iv) an outgoing data bus for transmitting data packets  
8 to the corresponding bus device, a method of arbitrating requests  
9 received from the N bus interfaces, the method comprising the steps  
10 of:

11                determining a first priority level associated with a  
12 first request packet received from a first bus device;

13                determining a second priority level associated with a  
14 second request packet received from a second bus device; and

15                comparing the first priority level and the second  
16 priority level to determine which of the first and second priority  
17 levels is higher.

1       18. The method as set forth in Claim 17 further comprising  
2 the step, in response to a determination that the first priority  
3 level is higher than the second priority level, of processing the  
4 first request packet prior to processing the second request packet.

1       19. The method as set forth in Claim 17 further comprising  
2 the step, in response to a determination that the first priority  
3 level is equal to the second priority level, of processing the  
4 first and second request packets on a rotating turn basis.

1       20. The method as set forth in Claim 17 further comprising  
2 the step of generating a current time slice value.

1       21. The method as set forth in Claim 20 further comprising  
2 the steps of:

3           determining a fixed time slice range associated with the  
4 first bus device; and

5           comparing the fixed time slice range with the current  
6 time slice value.

1        22. The method as set forth in Claim 21 further comprising  
2 the step, in response to a determination that the current time  
3 slice value is within the fixed time slice range, of processing the  
4 first request packet prior to processing the second request packet.

1        23. The method as set forth in Claim 22 further comprising  
2 the step, in response to a determination that the current time  
3 slice value is within the fixed time slice range, of processing the  
4 first request packet prior to processing any pending request packet  
5 received by the bus interface unit.